



STGF8NC60KD

N-channel 600V - 4A - TO-220FP
Short circuit rated PowerMESH™ IGBT

Features

Type	V _{CES}	V _{CE(sat)} Typ @25°C	I _C @100°C
STGF8NC60KD	600V	2.2V	4A

- Lower on voltage drop (V_{cesat})
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode
- Short circuit withstand time 10μs

Applications

- High frequency motor controls
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “K” identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

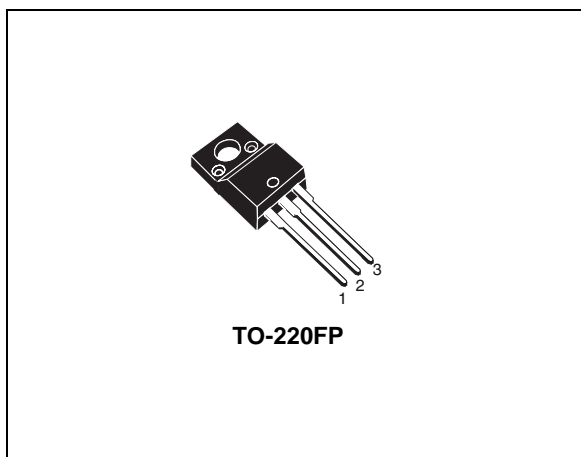


Figure 1. Internal schematic diagram

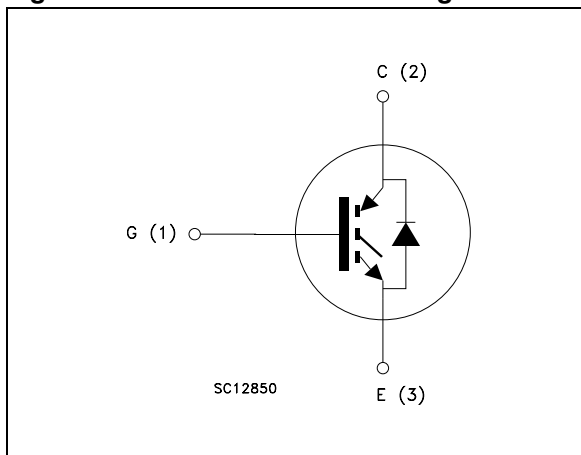


Table 1. Device summary

Order code	Marking	Package	Packaging
STGF8NC60KD	GF8NC60KD	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CES}	Collector-emitter voltage (V _{GS} = 0)	600	V
I _C ⁽¹⁾	Collector current (continuous) at T _C = 25°C	7	A
I _C ⁽¹⁾	Collector current (continuous) at T _C = 100°C	4	A
I _{CP} ⁽²⁾	Pulsed collector current	30	A
V _{GE}	Gate-emitter voltage	±20	V
I _F	Diode RMS forward current at T _C =25°C	7	A
I _{FSM}	Surge not repetitive forward current tp = 10ms sinusoidal	20	A
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;T _C =25°C)	2500	V
P _{TOT}	Total dissipation at T _C = 25°C	24	W
T _j	Operating junction temperature	- 55 to 150	°C
T _{scw}	Short circuit withstand time	10	µs

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max IGBT	5.1	°C/W
R _{thj-case}	Thermal resistance junction-case max diode	7	°C/W
R _{thj-amb}	Thermal resistance junction-ambient Max	62.5	°C/W

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	$I_C = 1\text{mA}, V_{GE} = 0$	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{V}, I_C = 3\text{A}$ $V_{GE} = 15\text{V}, I_C = 3\text{A}, T_C = 125^{\circ}C$		2.2 1.8	2.75	V V
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 250\ \mu\text{A}$	4.5		6.5	V
I_{CES}	Collector cut-off current ($V_{GE} = 0$)	$V_{CE} = \text{Max rating}, T_C = 25^{\circ}C$ $V_{CE} = \text{Max rating}, T_C = 125^{\circ}C$			150 1	μA mA
I_{GES}	Gate-emitter leakage current ($V_{CE} = 0$)	$V_{GE} = \pm 20\text{V}, V_{CE} = 0$			± 100	nA
g_{fs}	Forward transconductance	$V_{CE} = 15\text{V}, I_C = 3\text{A}$		15		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{V}, f = 1\text{MHz},$ $V_{GE} = 0$		380		pF
C_{oes}	Output capacitance			46		pF
C_{res}	Reverse transfer capacitance			8.5		pF
Q_g	Total gate charge	$V_{CE} = 390\text{V}, I_C = 3\text{A},$		19		nC
Q_{ge}	Gate-emitter charge	$V_{GE} = 15\text{V},$		5		nC
Q_{gc}	Gate-collector charge	(see Figure 18)		9		nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_J = 25^\circ C$ <i>(see Figure 19)</i>		17 6 655		ns ns A/ μs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_J = 125^\circ C$ <i>(see Figure 19)</i>		16.5 6.5 575		ns ns A/ μs
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V, I_C = 3A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_J = 25^\circ C$ <i>(see Figure 19)</i>		33 72 82		ns ns ns
$t_r(V_{off})$ $t_{d(off)}$ t_f	Off voltage rise time Turn-off delay time Current fall time	$V_{CC} = 390V, I_C = 3A,$ $R_{GE} = 10\Omega, V_{GE} = 15V,$ $T_J = 125^\circ C$ <i>(see Figure 19)</i>		60 106 136		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V, T_J = 25^\circ C$ <i>(see Figure 19)</i>		55 85 140		μJ μJ μJ
$E_{on}^{(1)}$ $E_{off}^{(2)}$ E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	$V_{CC} = 390V, I_C = 3A$ $R_G = 10\Omega, V_{GE} = 15V,$ $T_J = 125^\circ C$ <i>(see Figure 19)</i>		87 162 249		μJ μJ μJ

1. E_{on} is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	$I_f = 3A$		1.6	2.1	V
		$I_f = 3A, T_j = 125^\circ C$		1.3		V
t_{rr}	Reverse recovery time	$I_f = 3A, V_R = 30V,$ $T_j = 25^\circ C, di/dt = 100 A/\mu s$		23.5		ns
Q_{rr}	Reverse recovery charge	(see Figure 20)		16.5		nC
I_{rrm}	Reverse recovery current			1.4		A
t_{rr}	Reverse recovery time	$I_f = 3A, V_R = 30V,$ $T_j = 125^\circ C, di/dt = 100A/\mu s$		39		ns
Q_{rr}	Reverse recovery charge	(see Figure 20)		39		nC
I_{rrm}	Reverse recovery current			2		A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

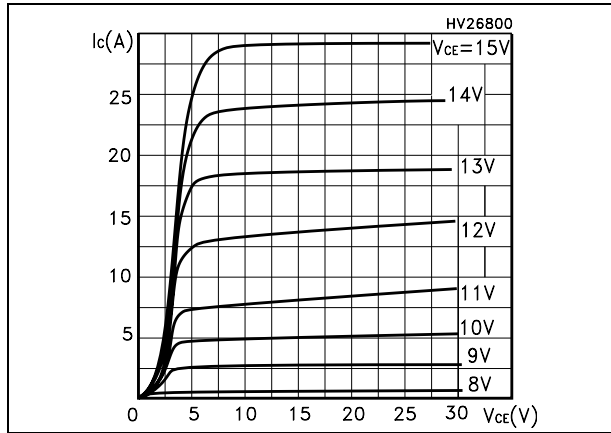


Figure 3. Transfer characteristics

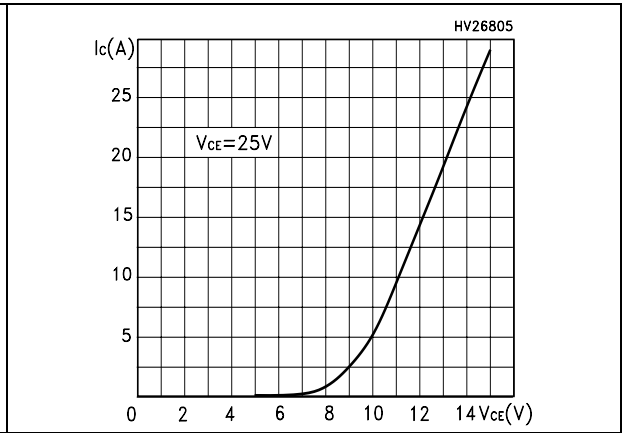


Figure 4. Transconductance

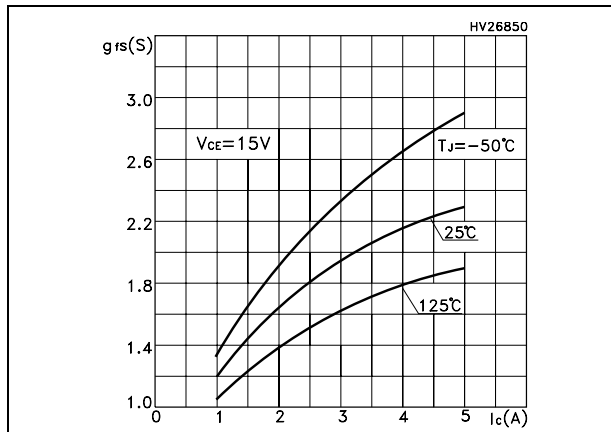


Figure 5. Collector-emitter on voltage vs temperature

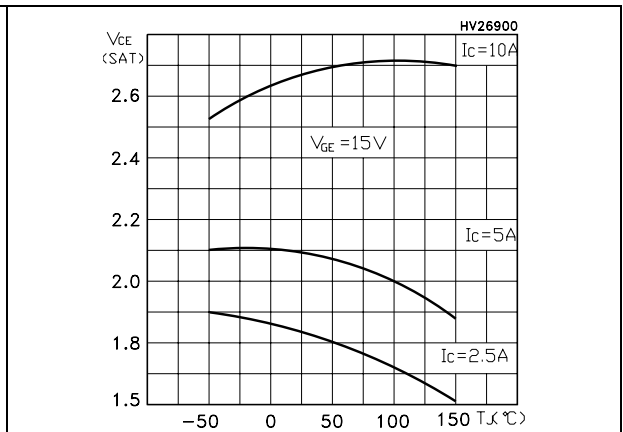


Figure 6. Gate charge vs gate-source voltage Figure 7. Capacitance variations

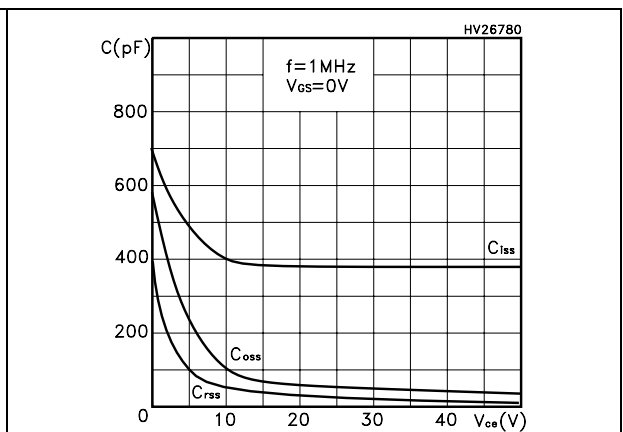
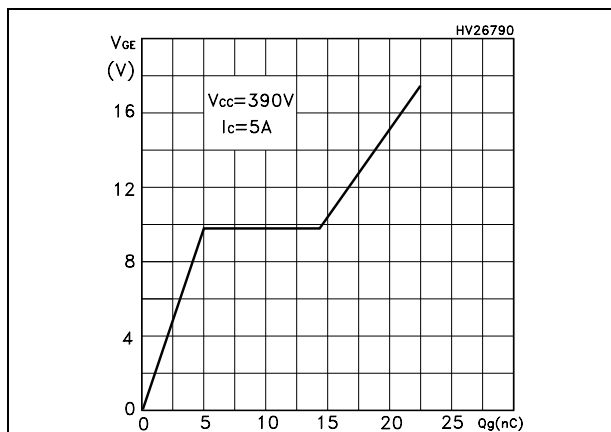


Figure 8. Normalized gate threshold voltage vs temperature

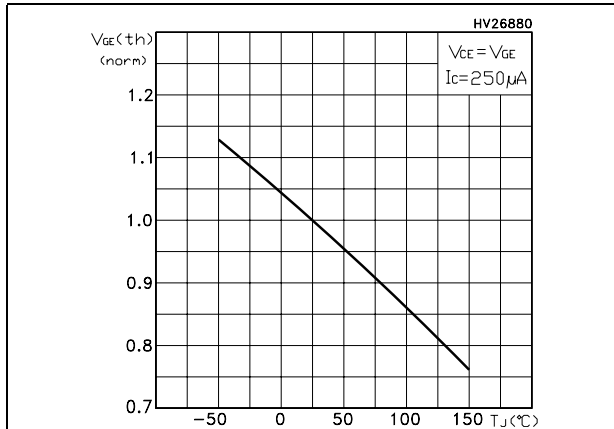


Figure 9. Collector-emitter on voltage vs collector current

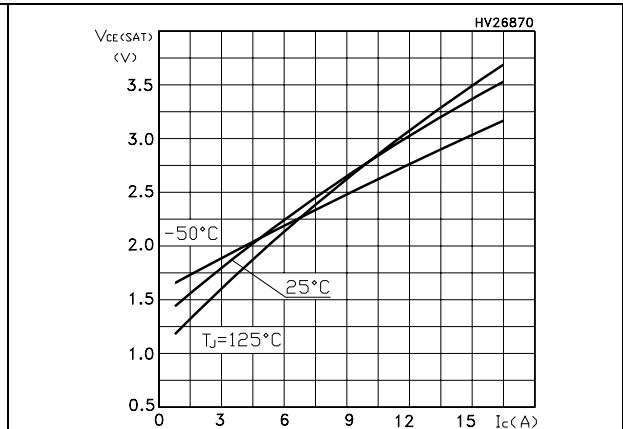


Figure 10. Normalized breakdown voltage vs temperature

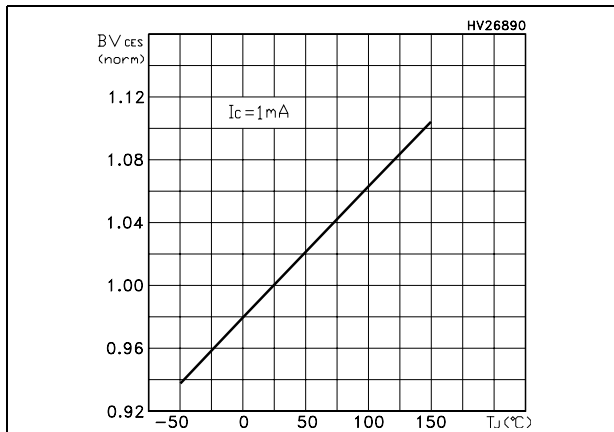


Figure 11. Switching losses vs temperature

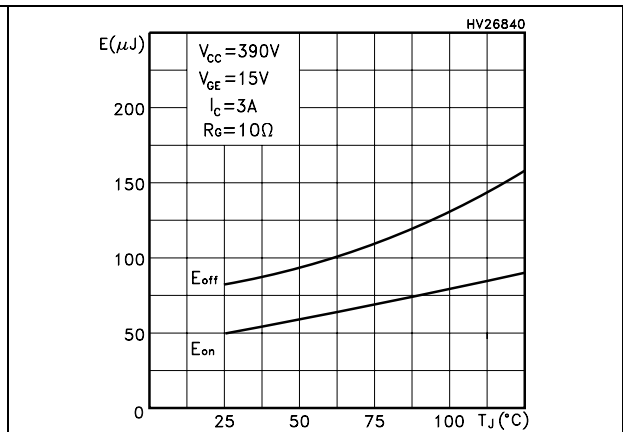


Figure 12. Switching losses vs gate resistance

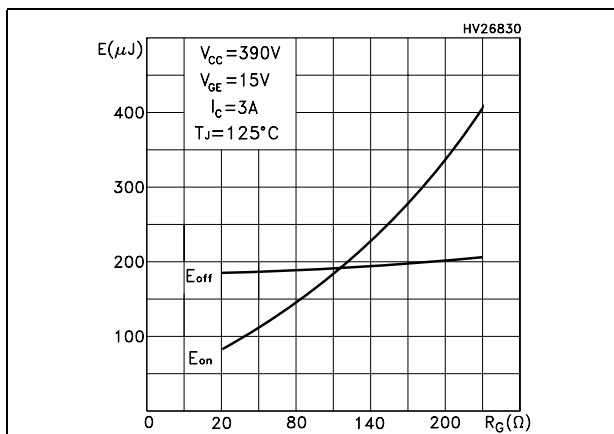


Figure 13. Switching losses vs collector current

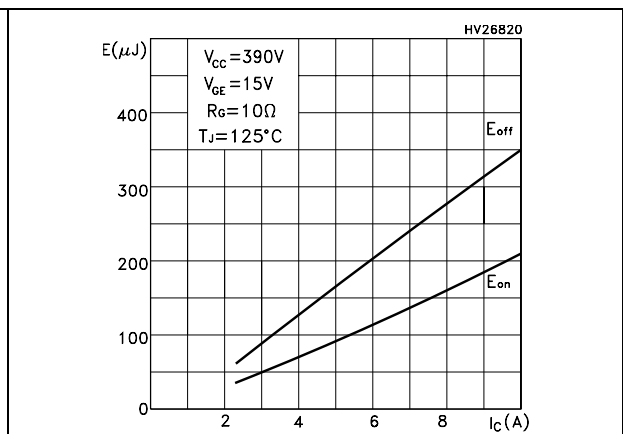


Figure 14. Thermal impedance

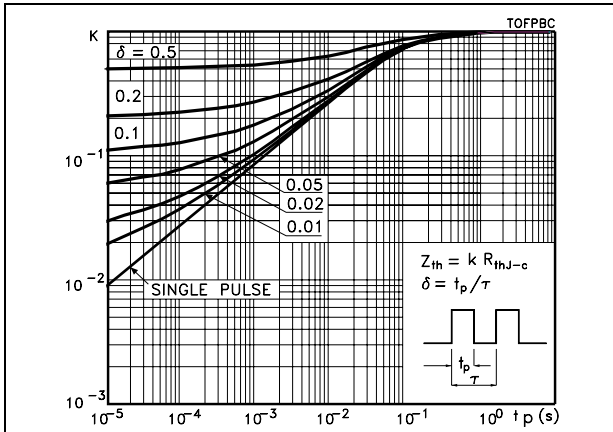


Figure 15. Turn-off SOA

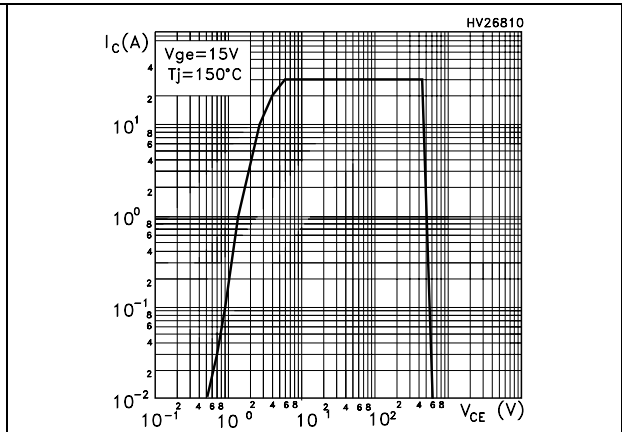
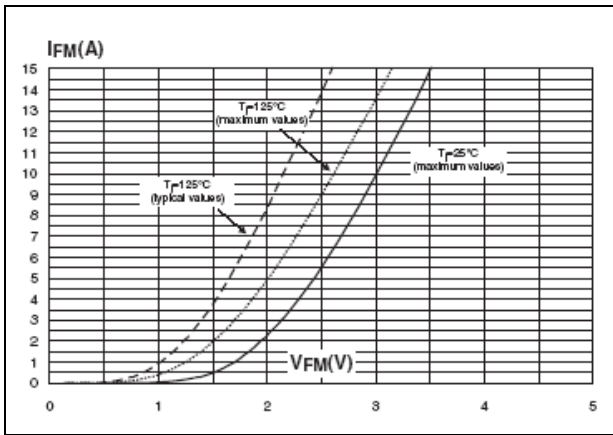


Figure 16. Forward voltage drop versus forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

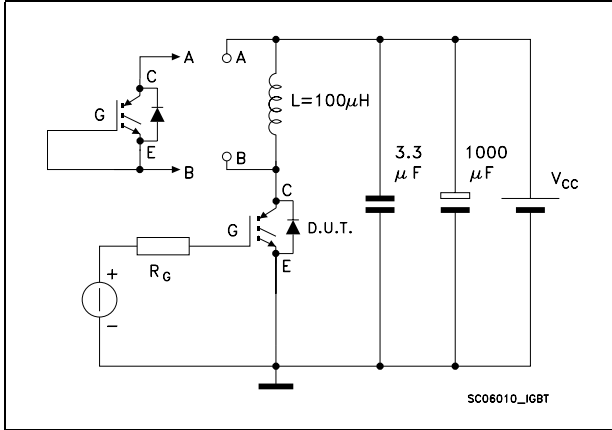


Figure 18. Gate charge test circuit

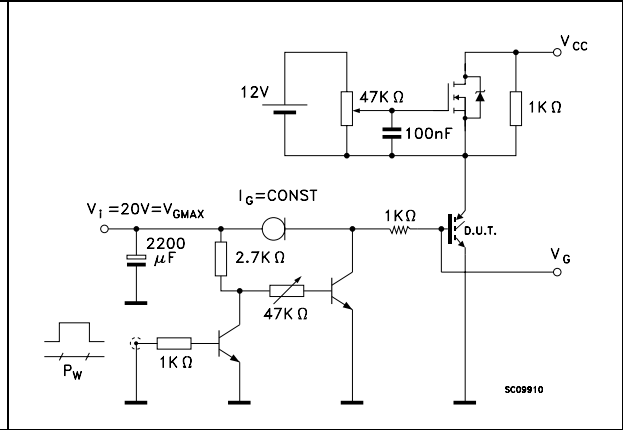


Figure 19. Switching waveform

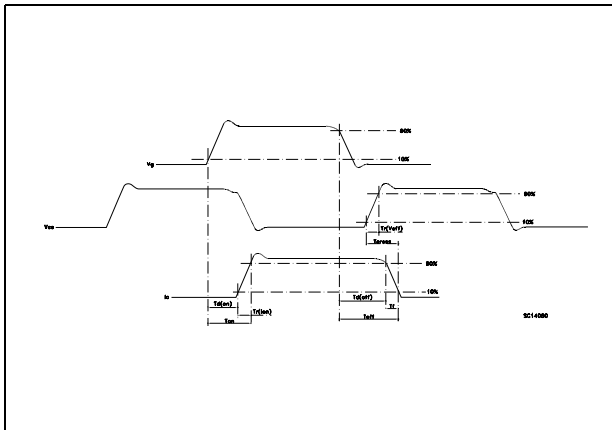
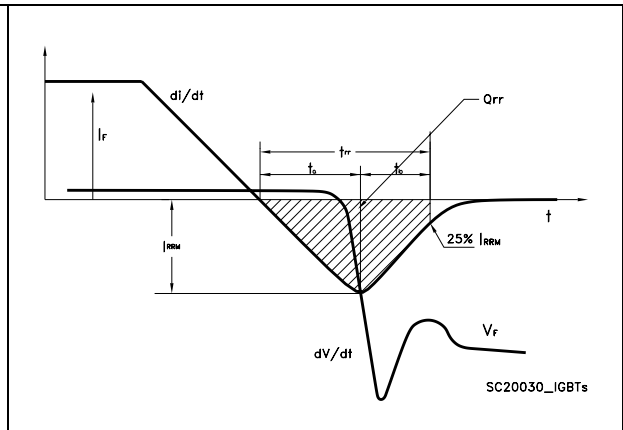


Figure 20. Diode recovery time waveform

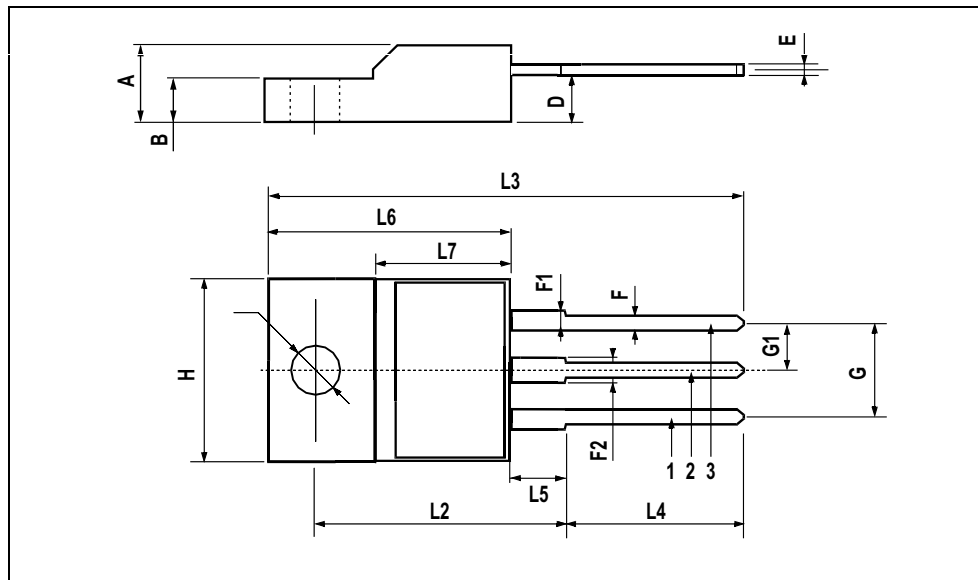


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Sep-2007	1	First release

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