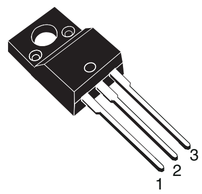
STGF8NC60KD

N-channel 600V - 4A - TO-220FP
Short circuit rated PowerMESH™ IGBT

Features

Type	V_{CES}	$V_{CE(sat)}$ Typ @25°C	I_C @100°C
STGF8NC60KD	600V	2.2V	4A

- Lower on voltage drop (V_{cesat})
- Lower C_{RES} / C_{IES} ratio (no cross-conduction susceptibility)
- Very soft ultra fast recovery antiparallel diode
- Short circuit withstand time 10µs



TO-220FP

Applications

- High frequency motor controls
- SMPS and PFC in both hard switch and resonant topologies
- Motor drivers

Description

Using the latest high voltage technology based on a patented strip layout, STMicroelectronics has designed an advanced family of IGBTs, the PowerMESH™ IGBTs, with outstanding performances. The suffix “K” identifies a family optimized for high frequency motor control applications with short circuit withstand capability.

Figure 1. Internal schematic diagram

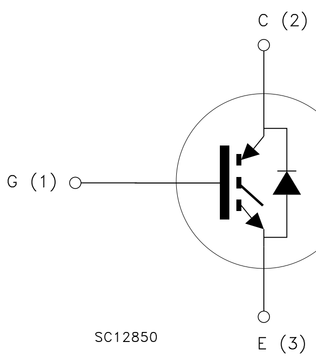


Table 1. Device summary

Order code	Marking	Package	Packaging
STGF8NC60KD	GF8NC60KD	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GS} = 0)	600	V
I_C(1)	Collector current (continuous) at T_C = 25°C	7	A
I_C(1)	Collector current (continuous) at T_C = 100°C	4	A
I_{CP}(2)	Pulsed collector current	30	A
V_{GE}	Gate-emitter voltage	±20	V
I_F	Diode RMS forward current at Tc=25°C	7	A
I_{FSM}	Surge not repetitive forward current tp = 10ms sinusoidal	20	A
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1s;Tc=25°C)	2500	V
P_{TOT}	Total dissipation at T_C = 25°C	24	W
T_j	Operating junction temperature	– 55 to 150	°C
T_{scw}	Short circuit withstand time	10	µs

1. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{JMAX} - T_C}{R_{THJ-C} \times V_{CESAT(MAX)}(T_C, I_C)}$$

2. Pulse width limited by max junction temperature

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max IGBT	5.1	°C/W
Rthj-case	Thermal resistance junction-case max diode	7	°C/W
Rthj-amb	Thermal resistance junction-ambient Max	62.5	°C/W

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR(CES)}$	Collector-emitter breakdown voltage	I_C= 1mA, V_{GE}= 0	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE}= 15V, I_C=3A V_{GE}= 15V, I_C= 3A, Tc= 125°C		2.2 1.8	2.75	V V
$V_{GE(th)}$	Gate threshold voltage	V_{CE}= V_{GE}, I_C= 250 µA	4.5		6.5	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE}= Max rating,T_C= 25°C V_{CE}=Max rating,T_C= 125°C			150 1	µA mA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE}= ±20V, V_{CE}= 0			±100	nA
g_{fs}	Forward transconductance	V_{CE} = 15V, I_C= 3A		15		S

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies} C_{oes} C_{res}	Input capacitance Output capacitance Reverse transfer capacitance	V_{CE} = 25V, f = 1MHz, V_{GE} = 0		380 46 8.5		pF pF pF
Q_g Q_{ge} Q_{gc}	Total gate charge Gate-emitter charge Gate-collector charge	V_{CE} = 390V, I_C = 3A, V_{GE} = 15V, *(see Figure 18)*		19 5 9		nC nC nC

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}= 15V, Tj= 25°C *(see Figure 19)*		17 6 655		ns ns A/µs
$t_{d(on)}$ t_r $(di/dt)_{on}$	Turn-on delay time Current rise time Turn-on current slope	V_{CC} = 390V, I_C =3A R_G= 10Ω, V_{GE}= 15V, Tj=125°C *(see Figure 19)*		16.5 6.5 575		ns ns A/µs
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{cc} = 390V, I_C = 3A, R_{GE} = 10Ω, V_{GE} =15V, T_J=25°C *(see Figure 19)*		33 72 82		ns ns ns
$t_r(V_{off})$ $t_d(_{off})$ t_f	Off voltage rise time Turn-off delay time Current fall time	V_{cc} = 390V, I_C = 3A, R_{GE}=10Ω, V_{GE} =15V, Tj=125°C *(see Figure 19)*		60 106 136		ns ns ns

Table 7. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}=15V, Tj=25°C *(see Figure 19)*		55 85 140		µJ µJ µJ
E_{on}(1) E_{off}(2) E_{ts}	Turn-on switching losses Turn-off switching losses Total switching losses	V_{CC} = 390V, I_C = 3A R_G= 10Ω, V_{GE}= 15V, Tj= 125°C *(see Figure 19)*		87 162 249		µJ µJ µJ

1. Eon is the turn-on losses when a typical diode is used in the test circuit in figure 2. If the IGBT is offered in a package with a co-pak diode, the co-pack diode is used as external diode. IGBTs & Diode are at the same temperature (25°C and 125°C)
2. Turn-off losses include also the tail of the collector current

Table 8. Collector-emitter diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_f	Forward on-voltage	I_f = 3A I_f = 3A, Tj = 125°C		1.6 1.3	2.1	V V
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 3A,V_R = 30V, Tj = 25°C, di/dt = 100 A/µs *(see Figure 20)*		23.5 16.5 1.4		ns nC A
t_{rr} Q_{rr} I_{rrm}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_f = 3A,V_R = 30V, Tj =125°C, di/dt = 100A/µs *(see Figure 20)*		39 39 2		ns nC A

2.1 Electrical characteristics (curves)

Figure 2. Output characteristics

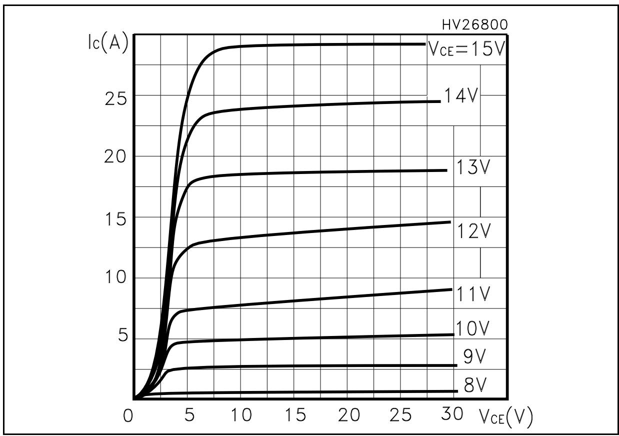


Figure 3. Transfer characteristics

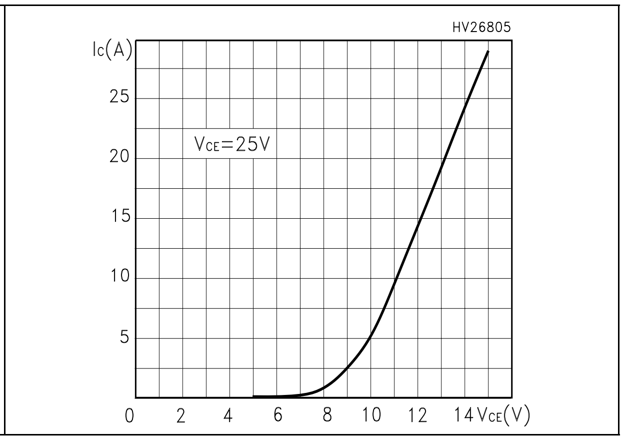


Figure 4. Transconductance

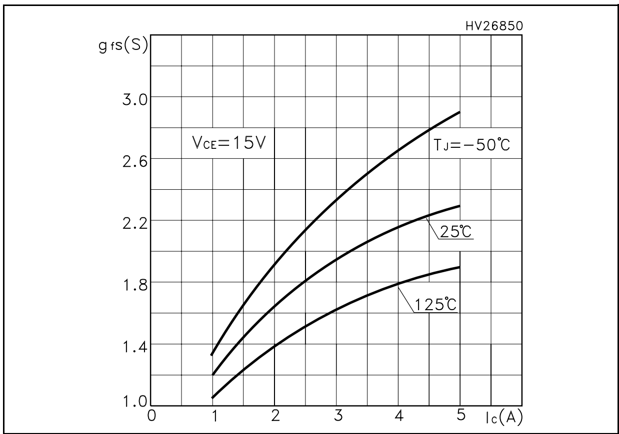


Figure 5. Collector-emitter on voltage vs temperature

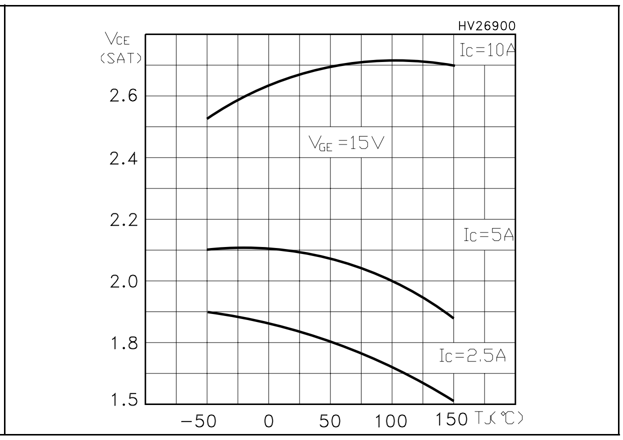


Figure 6. Gate charge vs gate-source voltage

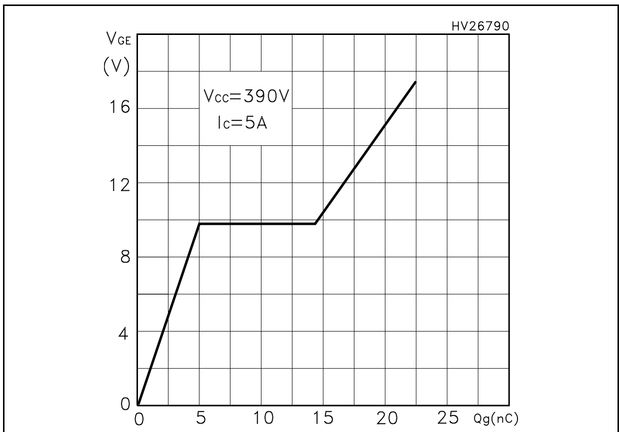


Figure 7. Capacitance variations

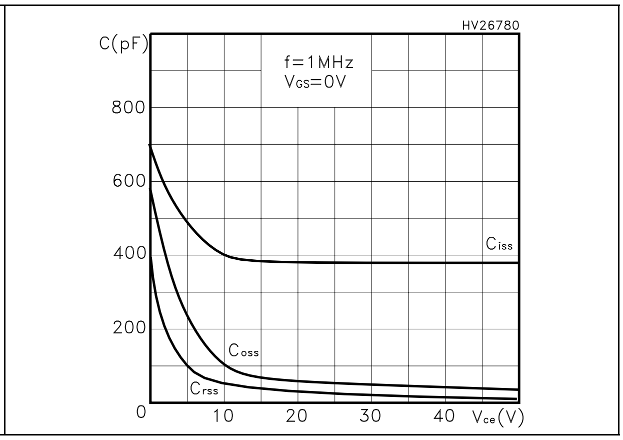


Figure 8. Normalized gate threshold voltage vs temperature

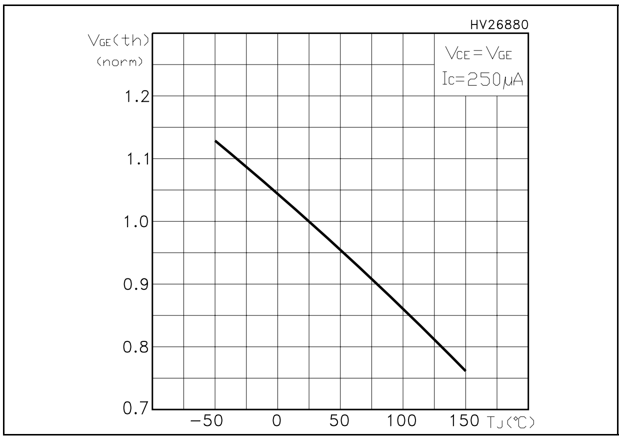


Figure 9. Collector-emitter on voltage vs collector current

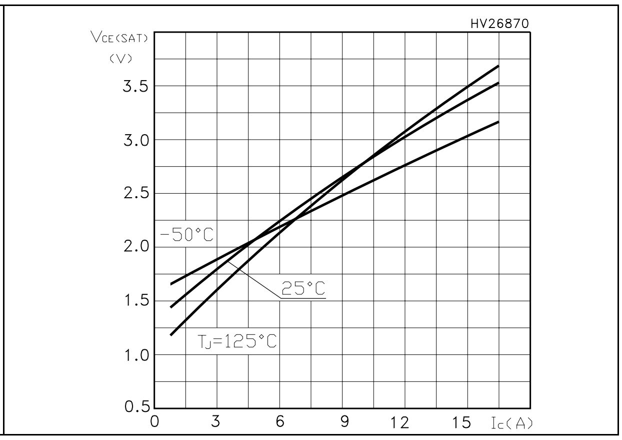


Figure 10. Normalized breakdown voltage vs temperature

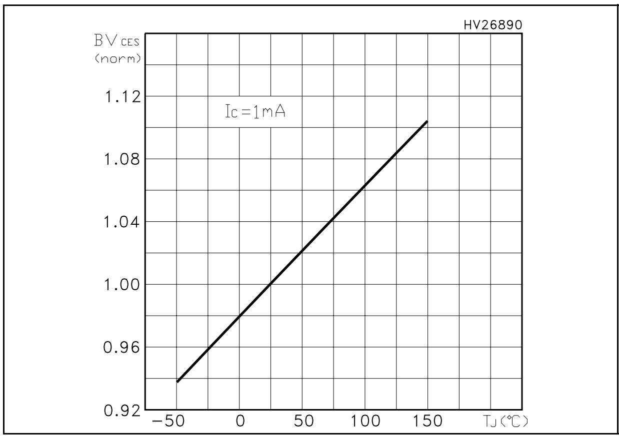


Figure 11. Switching losses vs temperature

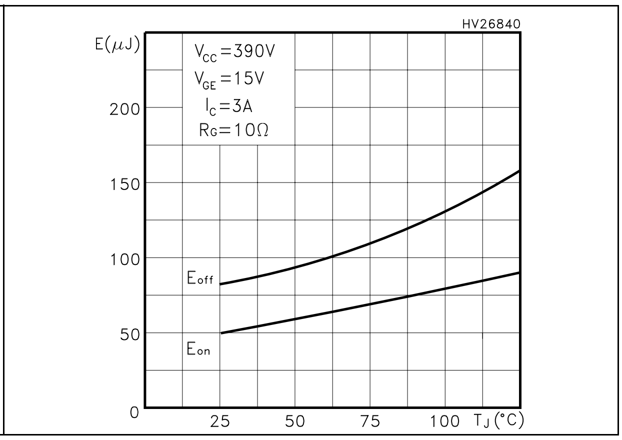


Figure 12. Switching losses vs gate resistance

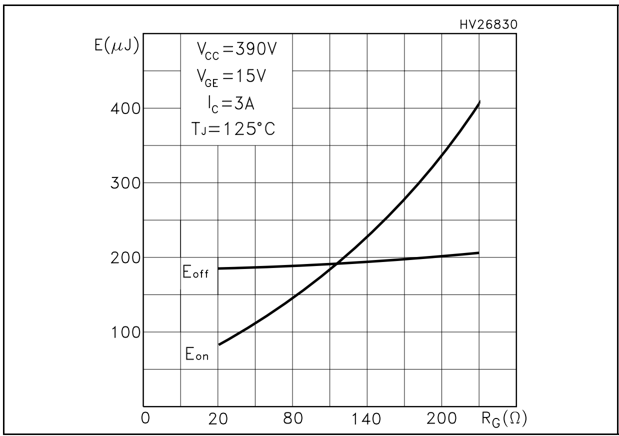


Figure 13. Switching losses vs collector current

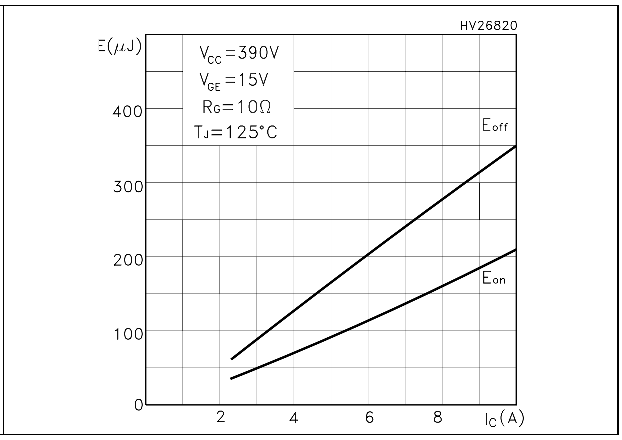


Figure 14. Thermal impedance

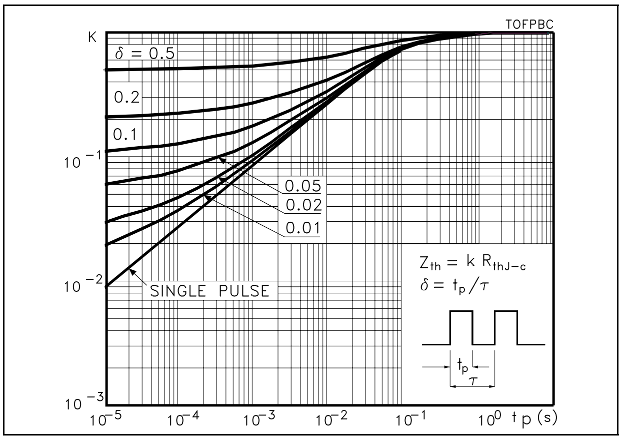


Figure 15. Turn-off SOA

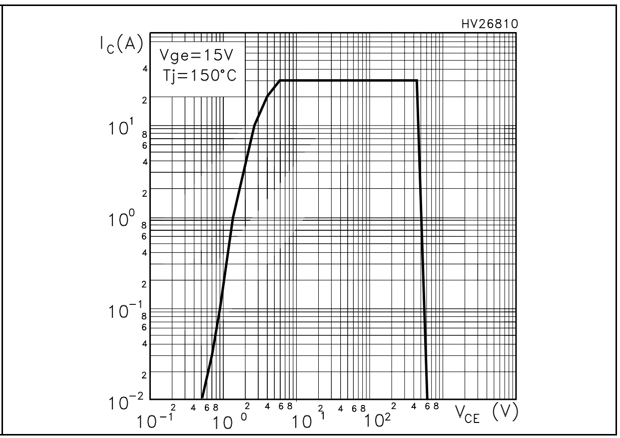
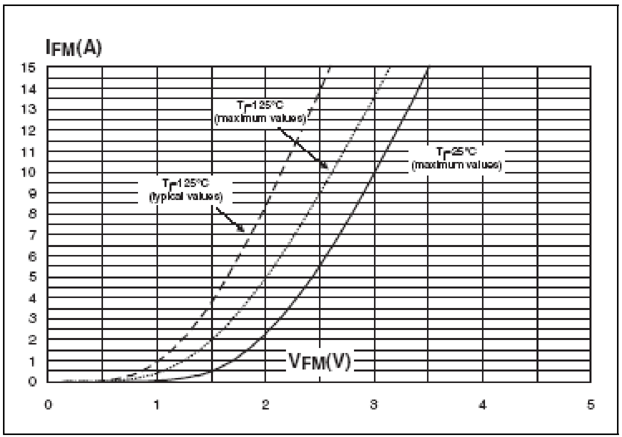


Figure 16. Forward voltage drop versus forward current



3 Test circuit

Figure 17. Test circuit for inductive load switching

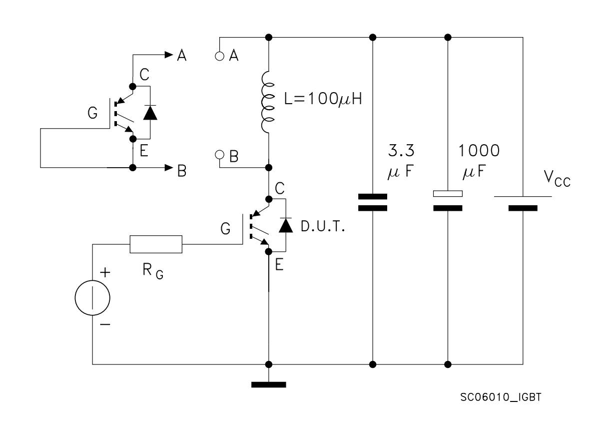


Figure 18. Gate charge test circuit

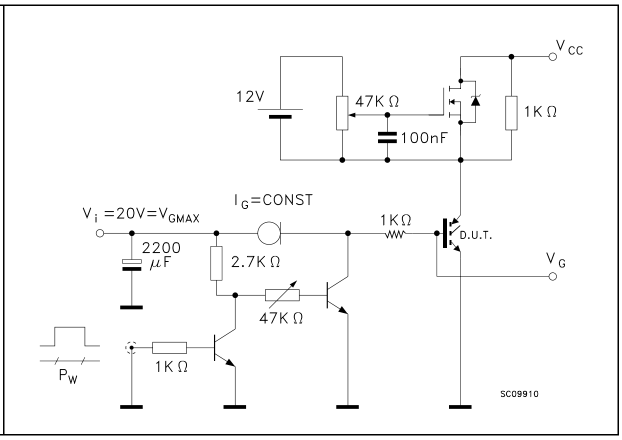


Figure 19. Switching waveform

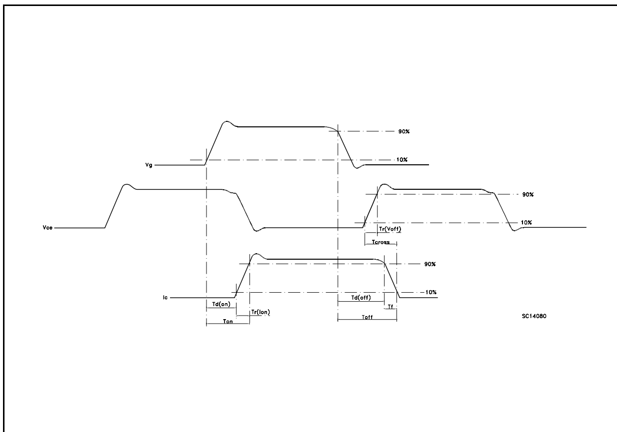
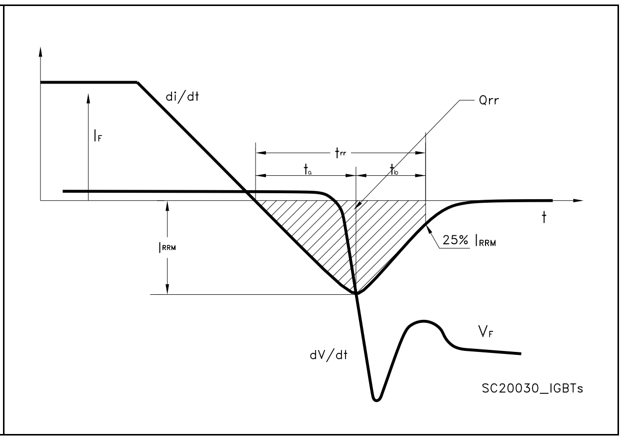


Figure 20. Diode recovery time waveform

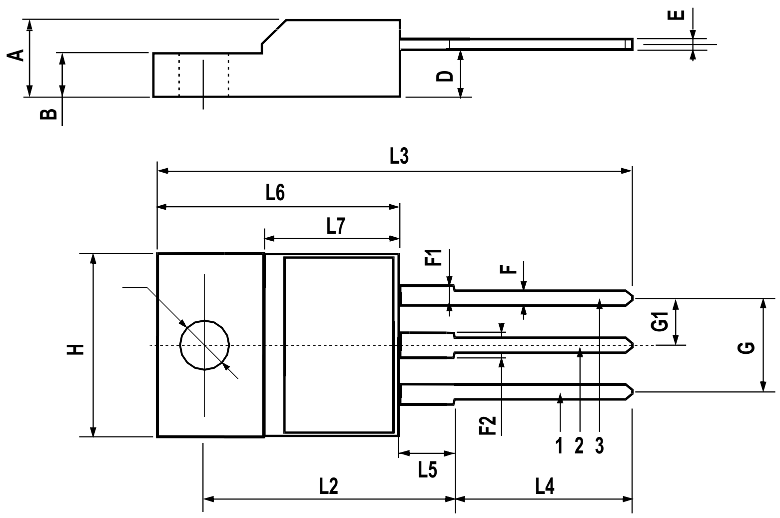


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
20-Sep-2007	1	First release